

Contents

1	Bio-Inspired Computational Intelligence for the Hardware of Adaptive Systems.....	1
1.1	Techniques of Computational Intelligence.....	1
1.2	Features and Classifications of Hybrid Intelligent Systems.....	9
1.3	Emergent Intelligent Technologies and the Adaptive Hardware Systems: AIS – A Technology for the Adaptive Systems.....	13
2	Advanced Hardware Implementation of the Computational Intelligence and Intelligent Technologies.....	27
2.1	Evolvable Hardware: An Overview.....	28
2.1.1	EHW Classification, Practical Engineering Remarks.....	30
2.1.2	EHW Technological Support (FPGA, FPAA, FPTA, FPMA, PsoC).....	37
2.1.2.1	Introduction to Programmable Integrated Circuits.....	38
2.1.2.2	FPGA Families and Advanced Type of FPGA.....	40
2.1.2.3	Field Programmable Analog Arrays(FPAA).....	44
2.1.2.4	Field Programmable Transistor Arrays (FPTA) Produced by NASA JPL.....	46
2.1.2.5	Practical Remarks on the Technological Support of EHW.....	48
2.1.3	EC Based Methods in EHW Implementation: EHW Architectures.....	50
2.1.4	An Application of GA for the Design of EHW Architectures.....	63
2.1.5	Global Remarks on Current Methods in EHW Technology and Its Prospectus.....	70
2.2	Hardware Implementation of the Artificial Immune Systems.....	73
2.3	Hardware Implementation of DNA Computing.....	75
2.4	Elements of Intercommunications Inside the AHS/EHW International Community (Conferences; Books; Journals; Elite Departments).....	76
3	Bio-Inspired Analogue and Digital Circuits and Their Applications.....	83
3.1	Introduction.....	83

3.2	Genetic Algorithms for Analogue Circuits Design.....	84
3.2.1	GA as Tools to Design Analogue Circuits.....	84
3.2.2	Overview of the Genetic Algorithm.....	86
3.2.3	Representation.....	89
3.2.4	Analogue Applications with FPTA Cells.....	91
3.2.5	Design Optimization of a CMOS Amplifier.....	92
3.2.5.1	Formulation of the Optimization Problem.....	92
3.2.5.2	Evaluation Engine.....	94
3.2.5.3	Optimization Engine.....	94
3.2.5.4	Design Optimization of a CMOS Amplifier.....	95
3.2.6	Evolving Software Models of Analogue Circuits.....	97
3.3	Evolutionary Design of Digital Circuits.....	99
3.3.1	Combinational Logic Circuits Evolutionary Design.....	99
3.3.2	Conventional Design Techniques for Arithmetic Adders and Multipliers.....	102
3.3.2.1	One Bit Full Adders.....	102
3.3.2.2	Parallel Processing Adder.....	105
3.3.2.3	CMOS Gates Full Adder.....	106
3.3.2.4	The Mirror Adder.....	107
3.3.2.5	Full Adder with CMOS Transmission Gates.....	107
3.3.2.6	Serial Processing Adder.....	109
3.3.2.7	Conventional Binary Multipliers.....	109
3.3.3	Arithmetic Circuits Designed with Evolutionary Algorithms.....	112
3.3.3.1	Full Adders Design.....	112
3.3.3.2	Gate-Level Evolutionary Design.....	114
3.3.3.3	Binary Multipliers Designed with Evolutionary Algorithms.....	116
3.3.4	Concluding Remarks on Digital Circuits Evolutionary Design.....	118
3.4	Reconfigurable Analogue Circuits in Mobile Communications Systems.....	119
3.4.1	Multi-standard Terminals for Mobile Telecommunications.....	119
3.4.2	Reconfigurable Multi-Standard Analogue Baseband Front-End Circuits in Mobile Communications Systems...	122
3.4.3	Reconfigurable RF Receiver Architectures.....	125
3.4.3.1	Superheterodyne Receiver.....	125
3.4.3.2	Direct - Conversion Architecture.....	126
3.4.3.3	Low IF Architecture.....	127
3.4.3.4	Software Defined Radio.....	127
3.4.3.5	Digital - IF Receiver.....	129
3.4.4	Fully Reconfigurable Analogue Filters Design.....	129
3.4.5	Reconfigurable Filter Stage for a Combined Zero-IF/Low-IF Radio Architecture.....	131
3.4.5.1	Flexible Zero-IF/Low-IF Radio Architecture.....	131

3.4.5.2	Transconductor-Based Reconfigurable and Programmable Analogue Array	133
3.4.5.3	Modular G_m -C State-Variable “Leapfrog” Filters.....	135
3.4.5.4	Simulation Results.....	139
3.4.5.5	Conclusions.....	140
3.4.6	Variable Gain Amplifiers.....	141
3.4.7	Genetic Algorithms for Reconfigurable Analogue IF Filters Design.....	146
3.5	Biomedical Engineering Applications.....	148
3.5.1	Electrical Stimulation and Neural Prosthesis.....	148
3.5.2	Cochlear Prosthesis via Telemetric Link.....	150
3.5.3	Reconfigurable Circuits in Implantable Auditory Prosthesis.....	151
3.5.4	AGCs in Auditory Prosthesis.....	153
3.5.5	Binary Controlled Variable Gain Amplifiers.....	156
3.5.5.1	Introduction.....	156
3.5.5.2	Digitally Controlled Gain Amplifier with Current Mirrors.....	156
3.5.5.3	Current Division Network.....	160
3.5.5.4	Programmable Amplifiers with CDN.....	162
3.5.5.5	Digitally Controlled Current Attenuator.....	165
3.6	Concluding Remarks.....	168
	References.....	169

