

Contents

Part I Model-Based System Specification Languages

1	Power and Energy Estimations in Model-Based Design	3
	Eric Senn, Saadia Douhib, Dominique Blouin, Johann Laurent, Skander Turki and Jean-Philippe Diguet	
1.1	Introduction	3
1.2	AADL Component Based Design Flow	5
1.3	Consumption Analysis: the Methodology	7
1.4	Power Estimation	8
1.4.1	Power Models	9
1.4.2	Multi-level Estimation	11
1.5	Power Estimation for Complex DSP	14
1.6	Power Estimation for Field Programmable Gate Array	16
1.7	Power Estimation for Operating System Services	17
1.7.1	Ethernet Communications Consumption Modelling	18
1.7.2	Models	19
1.8	Consumption Analysis Tool	20
1.8.1	Property Sets	20
1.9	Conclusion	23
	References	24
2	MARTE vs. AADL for Discrete-Event and Discrete-Time Domains	27
	Frédéric Mallet and Robert de Simone	
2.1	Introduction	27
2.2	Marte Time Model	28
2.2.1	Definitions	29
2.2.2	Event-Triggered Communications	29
2.2.3	Time-Triggered Communications	30
2.2.4	Periodic Tasks and Physical Time	31
2.2.5	TimeSquare	31
2.3	AADL	31
2.3.1	Modeling Elements	31
2.3.2	AADL Application Software Components	32
2.3.3	AADL Flows	33
2.3.4	AADL Ports	33
2.4	Three Different Configurations	34
2.4.1	The Aperiodic Case	34
2.4.2	The Mixed Event–Data Flow Case	37
2.4.3	The Periodic Case	38

2.5	Conclusion	39
	Glossary	40
	References	40
3	Generation of MARTE Allocation Models from Activity Threads . .	43
	Andreas W. Liehr, Klaus J. Buchenrieder, Heike S. Rolfs and Ulrich Nageldinger	
3.1	Introduction	43
3.2	Related Work	45
3.3	Building System Models with MARTE	46
3.4	Utilizing Activity Threads for Design Space Exploration	47
3.5	Generating MARTE Allocation Models with Activity Threads . . .	48
3.6	A Prototypic Implementation of the Method	51
3.7	Visualization of Performance Feedback	53
3.8	Summary and Outlook	54
	References	55
4	Model-Driven System Validation by Scenarios	57
	A. Carioni, A. Gargantini, E. Riccobene and P. Scandurra	
4.1	Introduction	57
4.2	ASMs and ASMETA	59
4.3	Scenario-Based Validation of ASM Models	60
	4.3.1 The AVALLA Language	60
4.4	The Model-Driven Validation Environment	61
	4.4.1 From SystemC UML Models to ASM Models	62
	4.4.2 Model Validator	64
4.5	The Simple Bus Case Study	64
4.6	Related Work	66
4.7	Conclusions and Future Work	68
	References	68
5	An Advanced Simulink Verification Flow Using SystemC	71
	Kai Hylla, Jan-Hendrik Oetjens and Wolfgang Nebel	
5.1	Introduction	71
5.2	Related Work	72
5.3	Extended Verification Flow	73
	5.3.1 Conventional Flow	73
	5.3.2 Extending the Verification Flow	76
5.4	Implementation	77
	5.4.1 Synchronization	77
	5.4.2 Data Type Conversion	80
5.5	Evaluation	80
	5.5.1 Implementation	80
	5.5.2 Extended Verification Flow	82

5.6 Conclusion 83
 References 84

Part II Languages for Heterogeneous System Design

6 VHDL–AMS Implementation of a Numerical Ballistic CNT Model 87
 Dafeng Zhou, Tom J. Kazmierski and Bashir M. Al-Hashimi
 6.1 Introduction 87
 6.2 Mobile Charge Density and Self-Consistent Voltage 88
 6.3 Numerical Piece-Wise Approximation of the Charge Density 89
 6.4 Performance of Numerical Approximations 91
 6.5 VHDL–AMS Implementation 93
 6.6 Conclusion 98
 References 99

7 Wide-Band Sigma–Delta ADC Design in Superconducting Technology 101
 R. Guelaz, P. Desgreys and P. Loumeau
 7.1 Introduction 101
 7.2 Sigma–Delta Second Order Architecture 102
 7.2.1 Bandpass Sigma–Delta Modulator 102
 7.2.2 The Josephson Junction 103
 7.2.3 The RSFQ Balanced Comparator 105
 7.2.4 Sigma Delta Modulator Operation with Josephson Junctions 105
 7.2.5 System Modeling with VHDL–AMS 106
 7.3 The Sigma–Delta ADC Design 107
 7.3.1 Clock and Comparator Design 107
 7.4 Simulation Results 109
 7.5 Conclusion 111
 References 112

8 Heterogeneous and Non-linear Modeling in SystemC–AMS 113
 Ken Caluwaerts and Dimitri Galayko
 8.1 Introduction 113
 8.1.1 SystemC–AMS Modeling Platform 114
 8.1.2 Summary of Electrostatic Harvester Operation 116
 8.2 SystemC–AMS Modeling of the Harvester 118
 8.2.1 Resonator Modeling 118
 8.2.2 Implementation of the Conditioning Circuit Model 119
 8.2.3 Model of the Whole System 123
 8.3 Modeling Results 124
 8.3.1 Description of the Modeling Experiment 124
 8.3.2 Modeling Results Validation 126
 8.4 Conclusion 127
 References 127

Part III Digital Systems Design Methodologies Based on C++

9	Application Workload and SystemC Platform Modeling for Performance Evaluation	131
	Jari Kreku, Mika Hoppari, Tuomo Kestilä, Yang Qu, Juha-Pekka Soininen and Kari Tiensyrjä	
9.1	Introduction	131
9.2	Performance Modeling and Simulation	133
9.2.1	Application and Workload Modeling	133
9.2.2	Execution Platform Modeling	134
9.2.3	Allocation and Transformation to SystemC	137
9.2.4	Performance Simulation	138
9.3	Mobile Video Player Case Example	138
9.3.1	Modeling of the Execution Platform Components	139
9.3.2	Modeling of the Services	141
9.3.3	Modeling of the Application	143
9.3.4	Analysis of Simulation Results	144
9.4	Conclusions	145
	References	146
10	Adaptive Interconnect Models for Transaction-Level Simulation	149
	Rauf Salimi Khaligh and Martin Radetzki	
10.1	Introduction	149
10.2	Related Work	151
10.3	Adaptive Interconnect Models	152
10.3.1	Point-to-Point Communication	152
10.3.2	Bus-Based Communication	154
10.4	Model Implementation	157
10.4.1	An Adaptive FSL Model	157
10.4.2	An Adaptive AHB Model	158
10.5	Experimental Results	160
10.6	Conclusion	164
	References	164
11	Efficient Architecture Evaluation Using Functional Mapping	167
	C. Kerstan, N. Bannow and W. Rosenstiel	
11.1	Introduction	167
11.1.1	Functional Mapping	168
11.1.2	Timing Behavior	169
11.2	Conventional Code Transformation	169
11.3	Optimization Approach	171
11.3.1	Class Unitized	171
11.4	Customize and Apply Unitized	173
11.4.1	Application of u_trace	174

- 11.5 Using the Approach in the Design Flow 175
 - 11.5.1 Handling Arrays 175
 - 11.5.2 Design Example 176
 - 11.5.3 Simulation Results 178
- 11.6 Limitations and Experiences 179
- 11.7 Summary 181
 - 11.7.1 Outlook 181
 - References 181
- 12 Symbolic Scheduling of SystemC Dataflow Designs 183**
 - Jens Gladigau, Christian Haubelt and Jürgen Teich
 - 12.1 Introduction 183
 - 12.2 Model of Computation 184
 - 12.3 Symbolic Representation 187
 - 12.4 QSS of SystemMoC Models 189
 - 12.4.1 Transition Graphs 190
 - 12.4.2 Path Searching 191
 - 12.4.3 Scheduling Algorithm 193
 - 12.5 Related Work 195
 - 12.6 Example 196
 - 12.7 Conclusions and Further Work 197
 - References 198
- 13 SystemC Simulation of Networked Embedded Systems 201**
 - Francesco Stefanni, Davide Quaglia and Franco Fummi
 - 13.1 Introduction 201
 - 13.2 The Architecture of SCNSL 203
 - 13.2.1 Main Components of SCNSL 204
 - 13.3 Main Problems Solved by SCNSL 207
 - 13.3.1 Simulation of RTL Models 207
 - 13.3.2 Assessment of Transmission Validity 207
 - 13.3.3 Simulation Planning 208
 - 13.3.4 Application to a Wireless Scenario 208
 - 13.4 Experimental Results 210
 - 13.5 Conclusions 210
 - References 211
- 14 Modeling of Embedded Software Multitasking in SystemC/OSSS . . . 213**
 - Philipp A. Hartmann, Philipp Reinkemeier, Henning Kleen and Wolfgang Nebel
 - 14.1 Introduction 213
 - 14.2 Related Work 214
 - 14.3 The OSSS Design Flow 216
 - 14.3.1 Application Layer 216
 - 14.3.2 Virtual Target Architecture Layer 217

14.4	Modeling Software in OSSS	218
14.4.1	Abstraction of Run-time System	218
14.4.2	Software Tasks	219
14.4.3	Software Shared Objects	220
14.4.4	Software Execution Times	221
14.5	Exploration of Platform Effects	222
14.6	Simulation Results	223
14.6.1	Accuracy and Performance	223
14.6.2	Lazy Synchronization	224
14.7	Conclusion	225
	References	225
15	High-Level Reconfiguration Modeling in SystemC	227
	Andreas Raabe and Armin Felke	
15.1	Introduction	227
15.2	Related Work	228
15.3	Basic Reconfiguration Modeling	229
15.3.1	Interpreting Reconfiguration as Circuit Switch	229
15.3.2	Creating Reconfigurable Modules from Static Ones	230
15.3.3	Control	231
15.4	Advanced ReChannel Features	231
15.4.1	Exportals	231
15.4.2	Synchronization	232
15.5	Explicit Description of Reconfiguration	233
15.5.1	Resettable Processes	234
15.5.2	Resettable Components	236
15.5.3	Binding Groups of Switches	237
15.6	Case Study	238
15.7	Conclusion and Future Work	239
	References	240
16	Stream Programming for FPGAs	241
	Franjo Plavec, Zvonko Vranesic and Stephen Brown	
16.1	Introduction	241
16.2	Stream Computing	243
16.2.1	Streaming on FPGAs	244
16.3	Compiling Brook to Hardware	244
16.3.1	Example Brook Program	246
16.3.2	Exploiting Data Parallelism	248
16.4	Experimental Evaluation	250
16.4.1	Results	251
16.5	Concluding Remarks	252
	References	253

Part IV Verification and Requirements Evaluation

17 A New Verification Technique for Custom-Designed Components at the Arithmetic Bit Level 257
 Evgeny Pavlenko, Markus Wedler, Dominik Stoffel, Wolfgang Kunz, Oliver Wienand and Evgeny Karibaev

17.1 Introduction 257

17.2 Normalization Method 259

 17.2.1 ABL Normalization 259

 17.2.2 Mixed ABL/Gate-Level Problems 262

17.3 Synthesis of ABL Descriptions from Gate-Level Models 263

 17.3.1 Generation of the Equivalent ABL Descriptions for Boolean Functions in Reed–Muller Form 264

17.4 Experimental Results 268

17.5 Conclusion and Future Work 271

 References 272

18 Debugging Contradictory Constraints in Constraint-Based Random Simulation 273
 Daniel Große, Robert Wille, Robert Siegmund and Rolf Drechsler

18.1 Introduction 273

18.2 SystemC Verification Library 275

18.3 Contradiction Analysis 276

 18.3.1 Problem Formulation 276

 18.3.2 Concepts for Contradiction Analysis 277

18.4 Implementation 280

18.5 Experimental Evaluation 282

 18.5.1 Types of Contradictions 283

 18.5.2 Effect of Property 1 and Property 2 284

 18.5.3 Real-Life Example 285

18.6 Conclusions 288

 References 289

19 Design of Communication Infrastructures for Reconfigurable Systems 291
 Alessandro Meroni, Vincenzo Rana, Marco D. Santambrogio and Francesco Bruschi

19.1 Introduction 291

19.2 Related Works 293

19.3 Real World Applications Analysis 293

 19.3.1 Applications Layer 294

 19.3.2 Scenarios Layer 295

 19.3.3 Characteristics Layer 295

 19.3.4 Metrics Layer 296

19.4 The Proposed Solution 297

 19.4.1 High Level Description 298

- 19.4.2 High Level Network Simulation 299
- 19.4.3 Evaluation and Selection 301
- 19.4.4 Verification and Validation 302
- 19.5 Results 302
- 19.6 Concluding Remarks 306
- References 306

- 20 Analysis of Non-functional Properties of MPSoC Designs 309**
Alexander Viehl, Björn Sander, Oliver Bringmann and Wolfgang
Rosenstiel
- 20.1 Introduction 309
- 20.2 Related Work 311
- 20.3 Preliminaries 312
 - 20.3.1 Activity Model 312
 - 20.3.2 Power Management Model 313
- 20.4 Design Flow 313
- 20.5 Abstraction of System Functionality 314
- 20.6 Simulation Model Generation 315
 - 20.6.1 Communication Dependency Graphs 315
 - 20.6.2 Temporal Environment Models 316
 - 20.6.3 Integration of Power Consumption and Power
Management 318
 - 20.6.4 Battery Models, Placement and Chip Environment 319
- 20.7 Experimental Results 320
- 20.8 Conclusions 322
- References 323